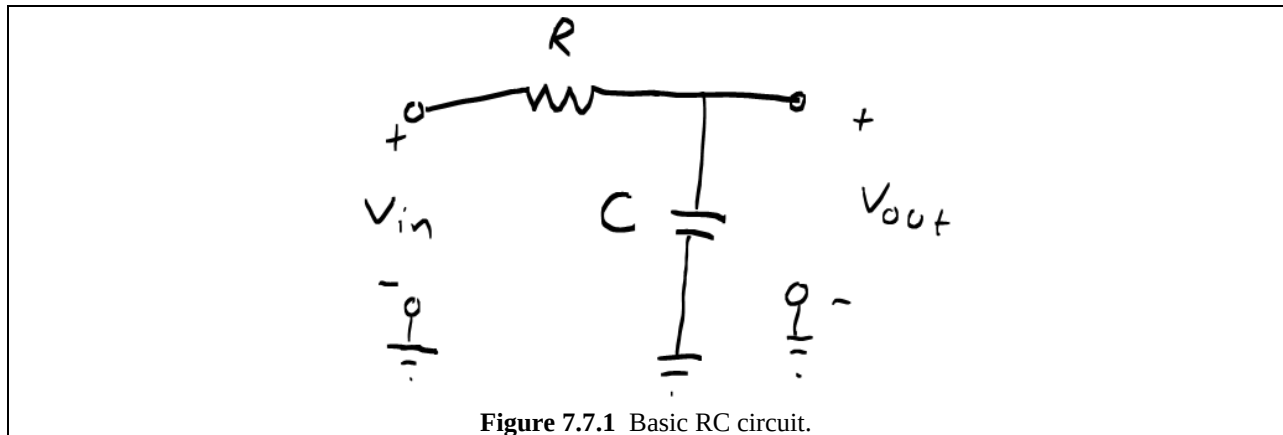


MULTISIM DEMO 7.7: THE LOGIC ANALYZER...AN INTRODUCTION

The Logic Analyzer in Multisim is an interesting tool because it allows us to see what dictates the value of the state of signals in the digital domain. In this demo, we'll briefly go over the mechanics of operating this instrument.

For this Demo, we want to measure how long it takes for three different RC circuits to charge up relative to one another. We will run the three circuits simultaneously in order to easily compare their responses. The three RC circuits follow the basic schematic shown in Fig. 7.7.1 below. The values for each circuit are as follows:

- Circuit 1: $R = 1\text{ k}\Omega$, $C = 10\text{ nF}$
 Circuit 2: $R = 1\text{ k}\Omega$, $C = 1\text{ nF}$
 Circuit 3: $R = 1\text{ k}\Omega$, $C = 100\text{ pF}$



Build the three RC circuits side by side and feed them an input signal from a CLOCK_VOLTAGE source which can be found under:

Group: Sources
 Family: SIGNAL_VOLTAGE_SOURCES
 Component: CLOCK_VOLTAGE

Once it is placed, double-click on the CLOCK_VOLTAGE source to bring up its control window and set its frequency (F) to 1 kHz, its Duty Cycle to 50, and its Voltage (V) to 5 V. This means that the signal will generate a square wave which goes from 0 to 5 V, spending equal time at each voltage with a period of 1 ms.

In addition to the three RC circuits and the source, insert a Logic Analyzer Instrument which can be found under Simulate>Instruments>Logic Analyzer or by pressing the  button on the instruments toolbar. Attach the outputs of the three RC circuits to the first three inputs of the Logic Analyzer as shown in Fig. 7.7.2 on the next page.

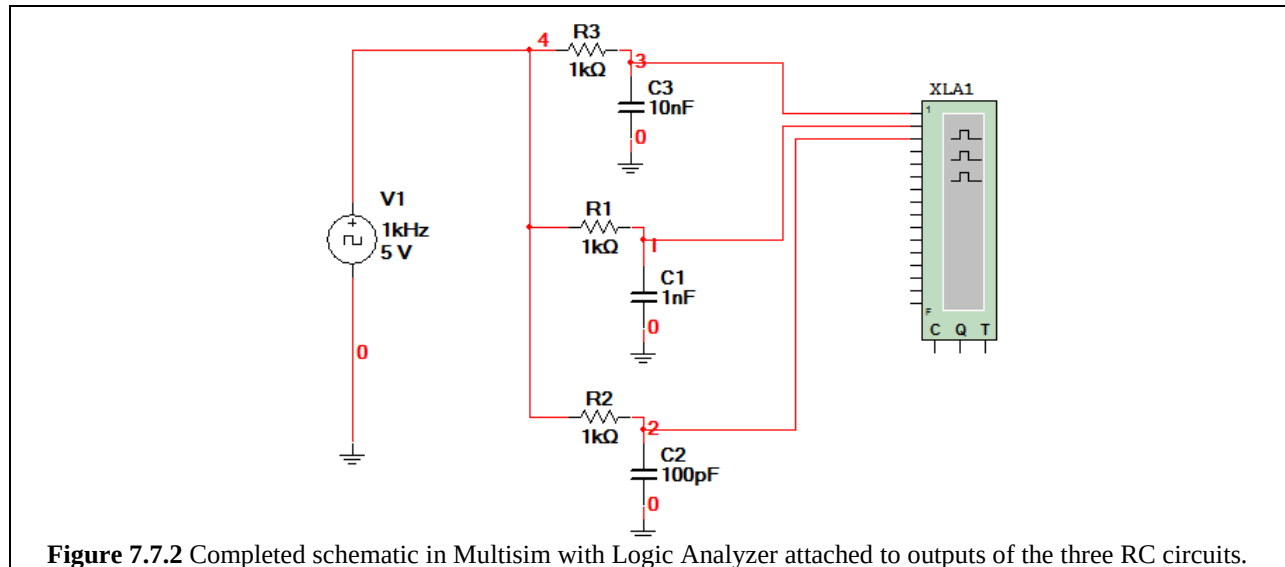


Figure 7.7.2 Completed schematic in Multisim with Logic Analyzer attached to outputs of the three RC circuits.

Now double click the Logic Analyzer instrument in order to open its control panel. At the bottom of the window, in the center, click on the “Set...” button. This will open up the window shown in Fig. 7.7.3.

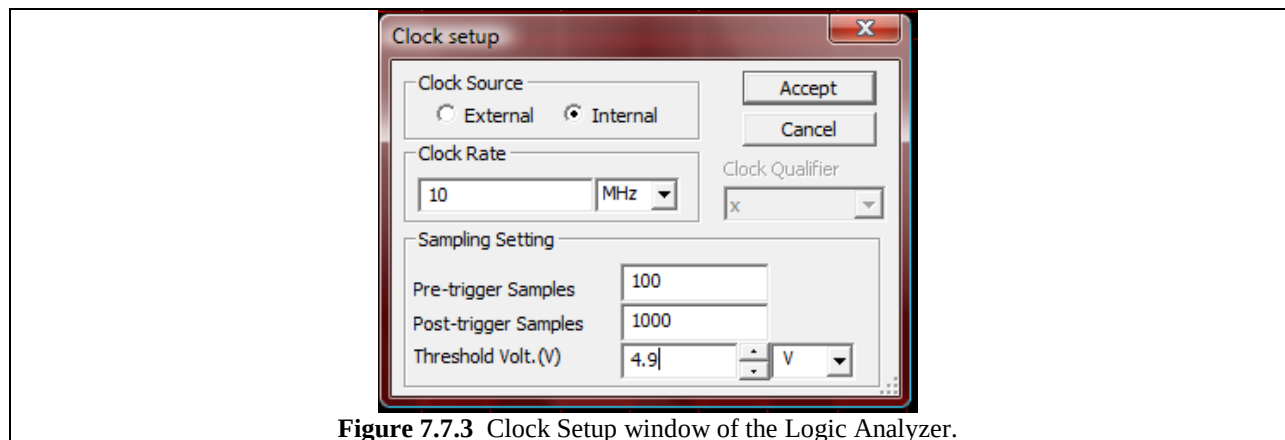


Figure 7.7.3 Clock Setup window of the Logic Analyzer.

We need to adjust a few parameters in this window in order for our simulation to run properly. First, leave the Clock Source on Internal. Second, set the clock rate to 10 MHz. This will guarantee a high-enough sample rate to pick up the differences in rise times between all three circuits. Third, adjust the Threshold Volt. (V) field to 4.9 V. The Threshold Voltage essentially defines what the Logic Analyzer sees as “Hi” voltage and “Lo” voltage or the binary 1 and 0, respectively. Voltages above 4.9 V are Hi, and voltages below 4.9 V are Lo. Naturally we want the Threshold Voltage to be set to a value which will be encountered in the simulation. If we set it at 6 V for our circuit, we’ll never get any Hi outputs because the maximum of the input signal is 5 V. So in all of your future endeavors with the Logic Analyzer keep this idea in mind. Leave the Pre-trigger Samples at 100 and leave the Post-trigger Samples at 1000. The Post-trigger Samples value dictates how long the instrument will sample data after we begin the simulation. Since the Clock rate is 10 MHz, corresponding to a period of 100 ns, 1000 post-trigger samples implies that the instrument will only collect data for 100 μ s ($100 \times 10^{-9} \cdot 1000$).

With all of these settings we've just applied, the logic analyzer will now be measuring how long it takes for each of the three RC circuits to charge up to 4.9 V. The Logic Analyzer assumes a reference of 0 V. As a result, we don't need to ground the instrument or give it a reference signal.

Now just like with any other Interactive Simulation Instrument in Multisim, you need to press F5 or the  to begin the progression of time, and consequently the measurement. The instrument should stop taking data at 100 μ s, even though the Interactive Simulation will continue to progress (as evidenced by the increasing time in the bottom right corner.) Scroll back to the beginning of the data recording using the arrows and scroll bar towards the bottom of the window, and your screen should look like Fig. 7.7.4 below.

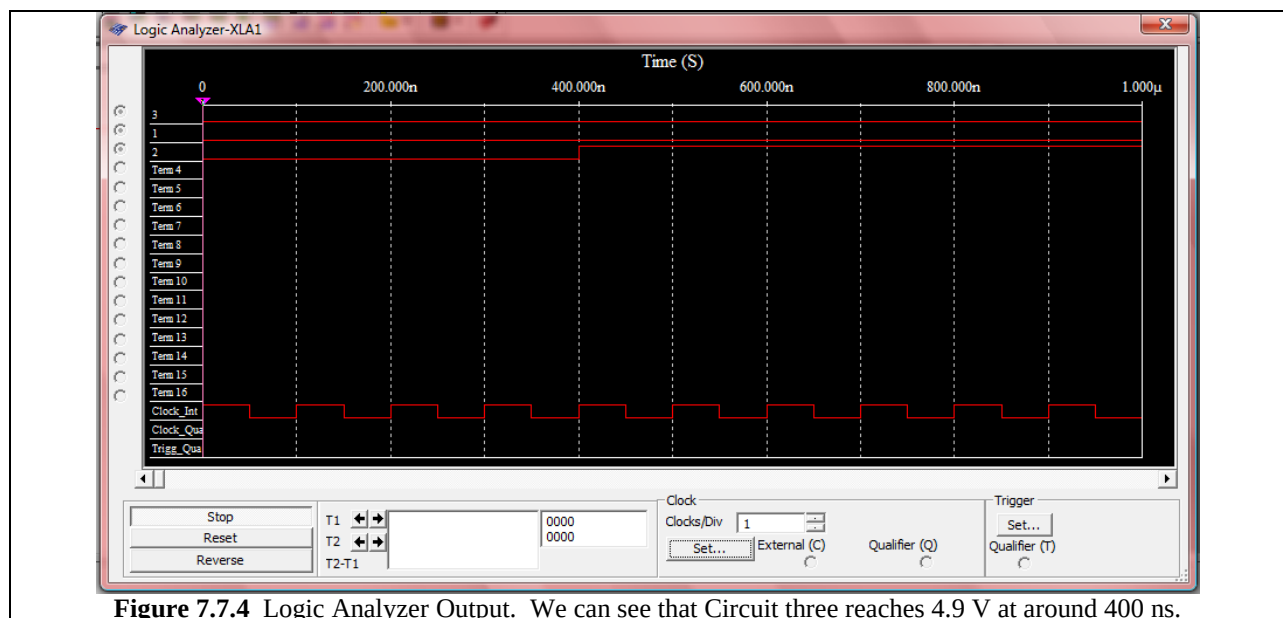
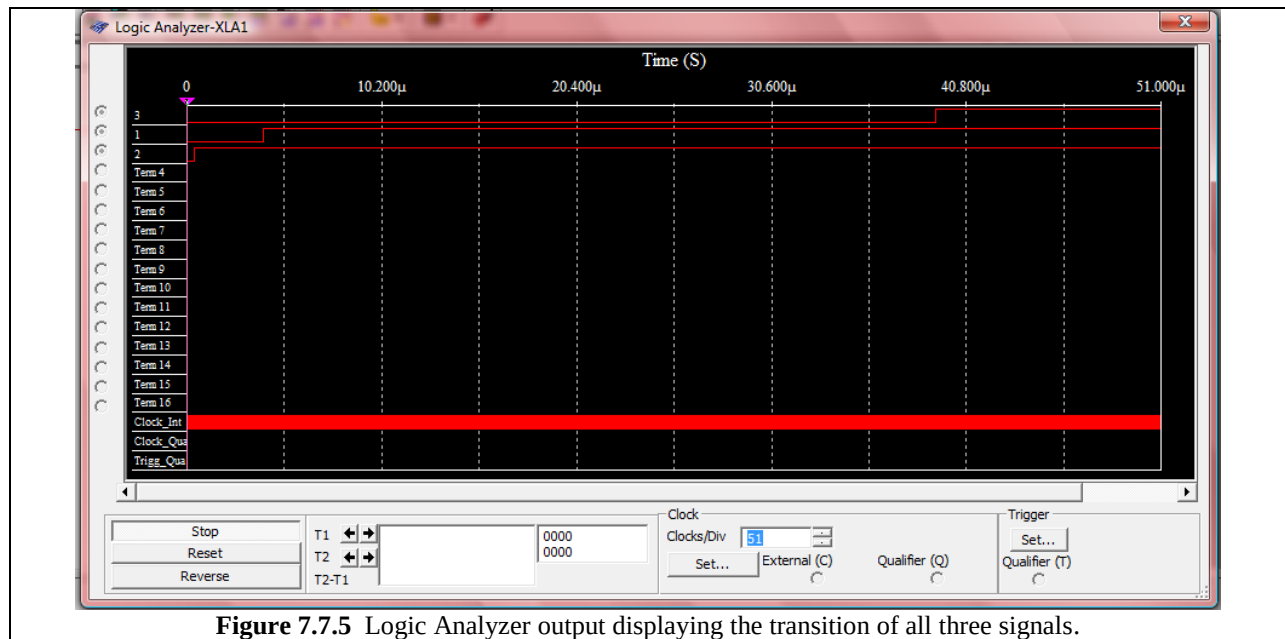


Figure 7.7.4 Logic Analyzer Output. We can see that Circuit three reaches 4.9 V at around 400 ns.

As we can see, all three signals start at a low state, but the third signal down, corresponding to Circuit 3 becomes Hi at 400 ns. The other two signals remain low to the end of the screen. They do rise eventually, but we can't really see them all that easily, because the Clocks/Div are too low. Each "Clock" has a period of $1/10\text{MHz} = 100\text{ ns}$. So we need to increase the number of Clocks/Div to a large value to see a larger range of time. When we increase Clocks/Div to 51, we get the plot shown in Fig. 7.7.5 on the next page.

Admittedly, increasing the Clocks/Div blurs the bottom Clock signal to a thick line, but now we can see all of the rises for the three signals of interest.

You may notice that the Input signals are labeled in a 3, 1, 2 descending fashion on the right side of the Logic Analyzer screen. Ignore this. The top signal corresponds with the top pin on the instrument symbol and the third signal down corresponds with the third pin on the instrument symbol.



Through using the cursors tucked on the left side of the output screen, we can see that the approximate differences between the times at which transition occurs are as follows:

Between Circuit 1 and Circuit 2: 35.205 μ s (top two traces)

Between Circuit 2 and Circuit 3: 3.616 μ s (bottom two traces)